THE INVENTION CLAIMED IS:

1. A data latch system comprising:

a data input for providing a first data bit having a first duration and a second data bit having a second duration, the first and second data bits having the same or opposite state;

a data output for providing the first data bit for the first and second durations;

first sampling circuitry connected to the data input and the data output for the first duration to provide the first data bit to the data output;

second sampling circuitry invertedly connected to the data input and connected to the data output for the second duration to provide the second data bit inverted to the data output; and

holding circuitry connected to the data output for the second duration whereby the holding circuitry holds the first data bit and the second sampling circuitry connects the second data bit inverted to the data output to enhance the held first data bit when the first and second data bits have different states.

2. The data latch system as claimed in claim 1 including clock circuitry connected to the first sampling circuitry, the second sampling circuitry, and the holding circuitry responsive to clock signals to establish the first and second durations.

3. The data latch system as claimed in claim 2 including a current source connected to the clock circuitry.

4. The data latch system as claimed in claim 1 including load circuitry connected to the first sampling circuitry, the second sampling circuitry, and the holding circuitry to provide pull-up loads therefor.

5. The data latch system as claimed in claim 1 wherein the gain ratio of the first sampling circuitry to the second sampling circuitry is greater than unity.

6. The data latch system as claimed in claim 1 including:

a second data latch system having a second data input, a third sampling circuitry connected to the second data input, a second data output connected to the third sampling circuitry, and a second holding circuitry connected to the second data output;

and wherein:

the data output is connected to the second data input and the second data output is isolated from the data input.

7. The data latch system as claimed in claim 6 including:

clock circuitry connected to the first sampling circuitry, the second sampling circuitry, and the holding circuitry responsive to clock signals to establish the first and second durations;

second clock circuitry connected to the third sampling circuitry and the second holding circuitry responsive to the clock signals to establish first and second durations for the second data latch system.

8. The data latch system as claimed in claim 1 including:

a demultiplexer input providing a plurality of sequential data bits;

a plurality of data latch systems, each of the plurality of data latch systems having:

a data input connected to the demultiplexer input,

a data output for providing each of the sequential data bits for successive times, and

first and second sampling circuitry and holding circuitry connected to the data input thereof whereby the holding circuitry holds the first of a pair of sequential data bits and the second sampling circuitry connects the second of the sequential pair of data bits to the data output to enhance the held first of the sequential pair of data bits when the first and second of the pair of sequential data bits have different states;

and wherein:

the data input is connected to the demultiplexer input; and

the data output provides a first of the plurality of sequential data bits for the first of the successive times.

9. The data latch system as claimed in claim 8 wherein:

the plurality of data latch systems each includes:

clock circuitry connected to the first sampling circuitry, the second sampling circuitry, and the holding circuitry responsive to clock signals to establish the first and second durations.

10. The data latch system as claimed in claim 9 wherein:

the data output provides the first of the plurality of sequential data bits for the first of the successive times in response to demultiplexer clock signals; and

the plurality of data latch systems provides the plurality of sequential data bits in response to the demultiplexer clock signals.

11. A data latch system comprising:

a differential data input for providing a first differential data bit having a first duration and a second differential data bit having a second duration, the first and second differential data bits having the same or opposite state;

a differential data output for providing the first differential data bit for the first and second durations;

first differential sampling circuitry connected to the differential data input and the differential data output for the first duration to provide the first differential data bit to the differential data output;

second differential sampling circuitry invertedly connected to the differential data input and connected to the differential data output for the second duration to provide the second differential data bit inverted to the differential data output; and

holding circuitry connected to the differential data output for the second duration whereby the holding circuitry holds the first differential data bit and the second differential sampling circuitry connects the second differential data bit to the differential data output to enhance the held first differential data bit when the first and second differential data bits have different states.

12. The data latch system as claimed in claim 11 including differential clock circuitry connected to the first differential sampling circuitry, the second differential sampling circuitry, and the holding circuitry responsive to differential clock signals to establish the first and second durations.

13. The data latch system as claimed in claim 12 including a current source connected to the differential clock circuitry.

14. The data latch system as claimed in claim 11 including load circuitry connected to the first differential sampling circuitry, the second differential sampling circuitry, and the holding circuitry to provide pull-up loads therefor.

15. The data latch system as claimed in claim 11 wherein the gain ratio of the first differential sampling circuitry to the second differential sampling circuitry is greater than unity.

16. The data latch system as claimed in claim 11 including:

a second data latch system having a second differential data input, a third differential sampling circuitry connected to the second differential data input, a second differential data output connected to the third differential sampling circuitry, and a second holding circuitry connected to the second differential data output;

and wherein:

the differential data output is connected to the second differential data input and the second differential data output is isolated from the differential data input.

17. The data latch system as claimed in claim 16 including:

differential clock circuitry connected to the first differential sampling circuitry, the second differential sampling circuitry, and the holding circuitry responsive to differential clock signals to establish the first and second durations;

second differential clock circuitry connected to the third differential sampling circuitry and the second holding circuitry responsive to the differential clock signals to establish first and second durations for the second differential data latch system.

18. The data latch system as claimed in claim 11 including:

a demultiplexer input providing a plurality of sequential data bits;

a plurality of data latch systems, each of the plurality of data latch systems having:

a data input connected to the demultiplexer input,

a data output for providing each of the sequential data bits for successive times, and

first and second sampling circuitry and holding circuitry connected to the data input thereof whereby the holding circuitry holds the first of a pair of sequential data bits and the second sampling circuitry connects the second of the sequential pair of data bits to the data output to enhance the held first of the sequential pair of data bits when the first and second of the pair of sequential data bits have different states;

and wherein:

the data input is connected to the demultiplexer input; and

the data output provides a first of the plurality of sequential data bits for the first of the successive times.

19. The data latch system as claimed in claim 18 wherein:

the plurality of data latch systems each includes:

clock circuitry connected to the first sampling circuitry, the second sampling circuitry, and the holding circuitry responsive to clock signals to establish the first and second durations.

20. The data latch system as claimed in claim 19 wherein:

the data output provides the first of the plurality of sequential data bits for the first of the successive times in response to demultiplexer clock signals; and

the plurality of data latch systems provides the plurality of sequential data bits in response to the demultiplexer clock signals.

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21. A data latch system comprising:

a differential data input for providing a first differential data bit having a first duration and a second differential data bit having a second duration, the first and second differential data bits having the same or opposite state;

a differential data output for providing the first differential data bit for the first and second durations;

first differential sampling circuitry connected to the differential data input and the differential data output for the first duration to provide the first differential data bit to the differential data output;

second differential sampling circuitry invertedly connected to the differential data input and connected to the differential data output for the second duration to provide the second differential data bit inverted to the differential data output;

holding circuitry connected to the differential data output for the second duration whereby the first differential sampling circuitry provides the first differential bit during the first duration and the holding circuitry holds the first differential data bit and the second differential sampling circuitry connects the second differential data bit to the differential data output to enhance the held first differential data bit during the second duration when the first and second differential data bits have different states;

first differential clock circuitry connected to the first differential sampling circuitry and the holding circuitry; and

second differential clock circuitry connected to the first differential sampling circuitry and the second differential sampling circuitry whereby the first differential clock circuitry and the second differential clock circuitry respond to differential clock signals to establish the first and second durations.

22. The data latch system as claimed in claim 21 including:

a current source connected to the differential clock circuitry; and

load circuitry connected to the first differential sampling circuitry, the second differential sampling circuitry, and the holding circuitry to provide pull-up loads therefor.

23. The data latch system as claimed in claim 21 wherein the gain ratio of the first differential sampling circuitry to the second differential sampling circuitry is about three.

24. The data latch system as claimed in claim 21 including:

a second data latch system having a second differential data input, a third differential sampling circuitry connected to the second differential data input, a second differential data output connected to the third differential sampling circuitry, a second holding circuitry connected to the second differential data output and second differential clock circuitry connected to the third differential sampling circuitry and the second holding circuitry responsive to the differential clock signals to establish first and second durations for the second differential data latch system;

and wherein:

the differential data output is connected to the second differential data input and the second differential data output is isolated from the differential data input.

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25. The data latch system as claimed in claim 21 including:

a demultiplexer input providing a plurality of sequential differential data bits;

a plurality of data latch systems, each of the plurality of data latch systems having:

a differential data input connected to the demultiplexer input,

a differential data output for providing each of the plurality of sequential differential data bits for successive times,

first and second differential sampling circuitry and holding circuitry connected to the differential data input thereof whereby the holding circuitry holds the first of the plurality of sequential differential data bits and the second differential sampling circuitry connects the second of the plurality of sequential differential data bits to the differential data output to enhance the held first of the plurality of sequential differential data bits when the first and second of the plurality of sequential differential data bits have different states, and

differential clock circuitry connected to the first differential sampling circuitry, the second differential sampling circuitry, and the holding circuitry responsive to clock signals to establish the first and second durations;

and wherein:

the differential data input is connected to the demultiplexer input; and

the differential data output provides a first of the plurality of sequential differential data bits for the first of the successive times.

26. The data latch system as claimed in claim 25 wherein:

the data output provides the first of the plurality of sequential differential data bits for the first of the successive times in response to demultiplexer clock signals; and

the plurality of data latch systems provides the plurality of sequential differential data bits in response to the demultiplexer clock signals.